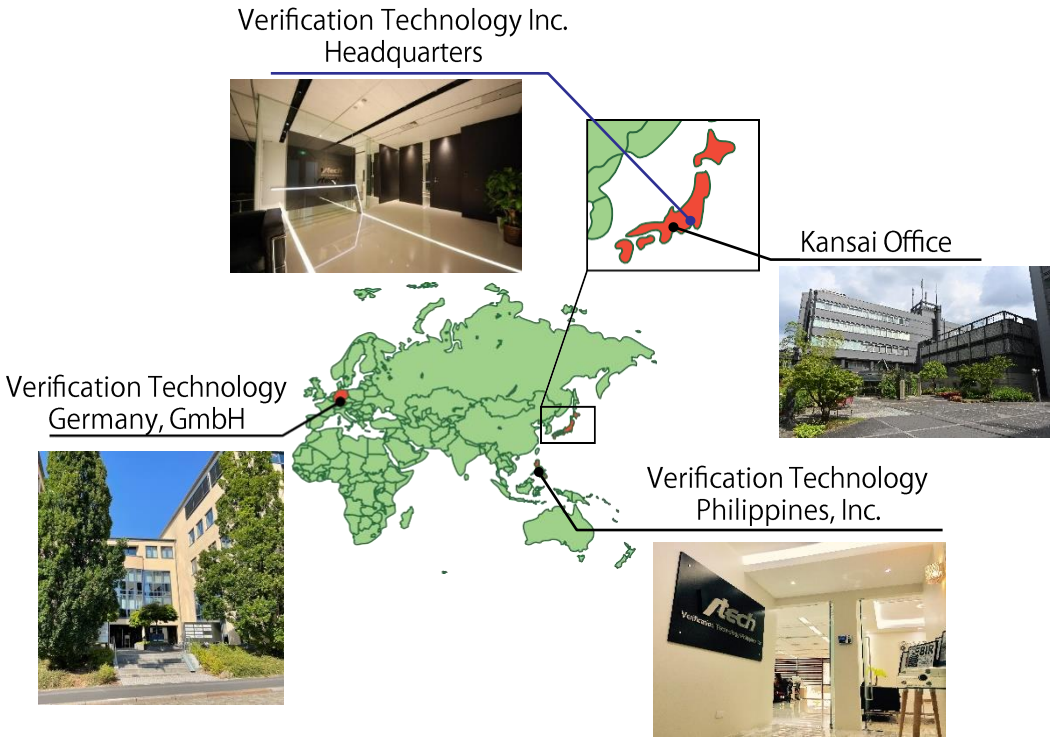
Name	**Verification Technology, Inc. (Vtech)**
Establish	April 1st, 2003
CEO	Hideto Takeuchi
Fund	JPY 60,550,000
Business Solution	◆LSI Design & Verification Services ◆Functional Safety Services ◆Medical Device Certification Support Services
Location	◆ Headquarters 5F Shin-Yokohama Square Bldg., 2-3-12 Shin-Yokohama Kohoku-ku, Yokohama-shi, Kanagawa, 222-0033 Japan Tel :+81-45-470-8310 Fax:+81-45-470-8319 ◆ Kansai Branch Room No. 202, 2F KRP2-2gokan, 134 Chudojiminamimachi Shimogyo-ku, Kyoto-shi, Kyoto, 600-8813 Japan Tel :+81-75-950-0430 Fax:+81-75-950-0431 ◆ Verification Technology Germany, GmbH Bamberger Strasse 7, 01187 Dresden, Germany ◆ Verification Technology Philippines, Inc (Engeneering center) UG15 Upper Ground Cityland Pasong Tamo, 6264 Calle Estacion St., Makati City Philippines



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https://www.vtech-global.com/

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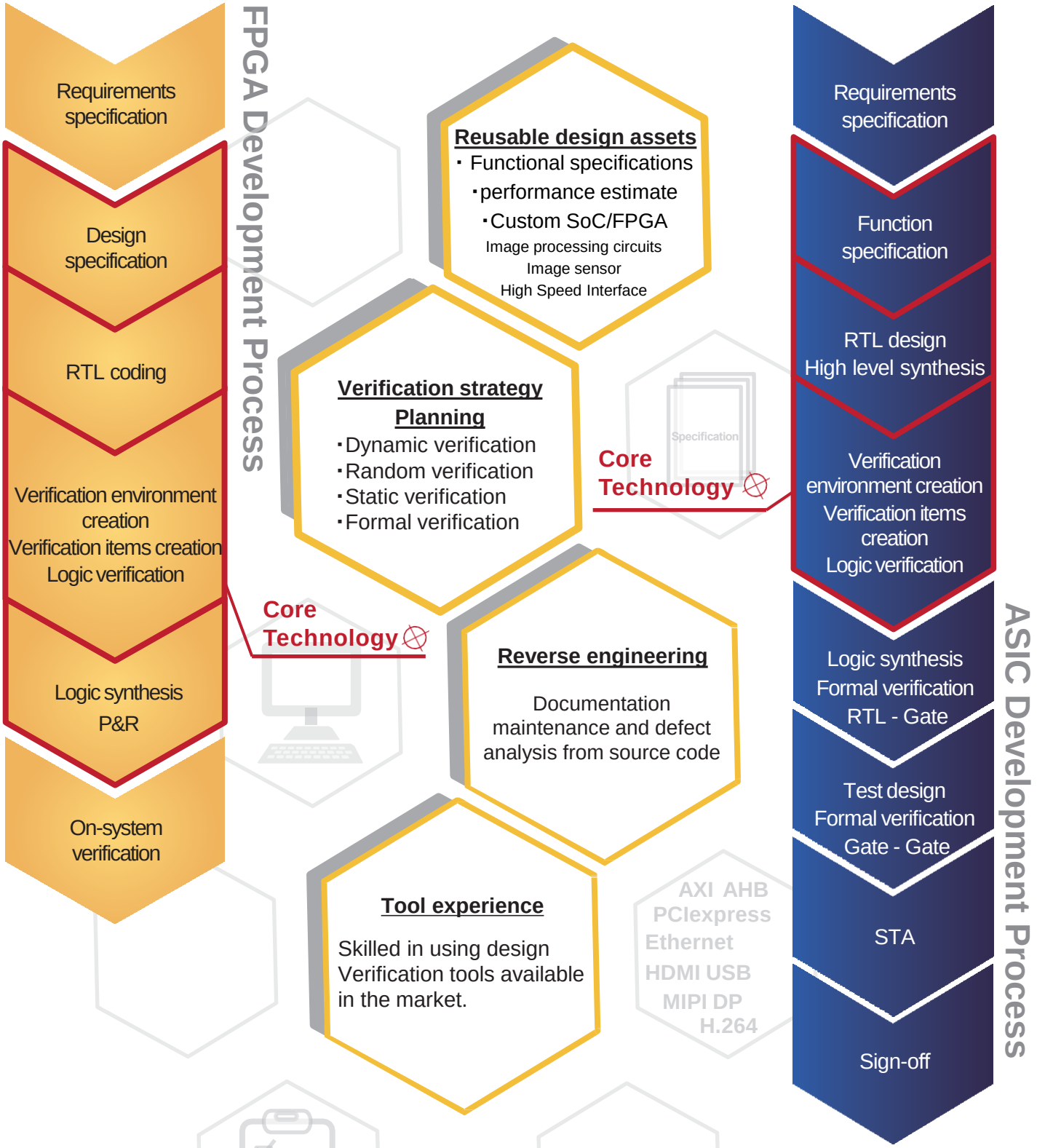

Tools

Tool Name		Vendor	Licensed(※1)
Simulator	Xcelium	Cadence	○
	Questasim	Siemens	○
	VCS	Synopsys	○
CDC	JasperCDC	Cadence	
	QuestaCDC	Siemens	○
	SpyGlassCDC	Synopsys	
Formal	JasperGold	Cadence	
	QuestaFormal	Siemens	○
	VC Formal	Synopsys	

Tool Name		Vendor	Licensed(※1)
Lint	HAL	Cadence	
	QuestaLint	Siemens	○
	SpyGlassLint	Synopsys	
FPGA Development	QuartusPrime	Intel	○
	VivadoML(※2)	Xilinx	○
High Level Synthesis	StratusHLS	Cadence	
	Catapult	Siemens	
	CyberWorkBench	NEC	
Other	Z01X	Synopsys	

(※1) We have a track record of using many tools that we don't licensed. We have also used emulators and VIPs.
(※2) High Level Synthesis Tools is VitisHLS.

Application	Customer product	Development contents	Vtech's scope of work
Imaging Processor	**Electronic image stabilization LSI**	Application I/F controller CIS data receiver processing Memory sub-system (IP implementation) System synchronizing controller	RTL design & verification System C design & high level synthesis
	Mirrorless single lens reflex camera	HDR synthesis	System C design & high level synthesis ASIC RTL design & verification
		Imaging peripheral circuits Image processing circuits (incl. JPEG compression/decompression)	ASIC RTL design & verification Verification with emulator (Palladium)
	High speed camera	Pixel interpolation	FPGA RTL design & verification
Medical	**Digestive organs endoscope**	Light source Control FPGA Development	RTL design & verification
		Image processing IP development	RTL design & verification (Stratix/Kintex-Ultrascale+)
		Chip level simulation environment for large scale FPGA	Input/output model development Memory model development (dynamic memory) System control/debug mechanism development
	Medical film printer	FPGA development	Reverse engineering RTL design/Verification environment creation/Verification; FPGA implementation On-system verification
Communication	**5G communication devices**	Optimization of scheduler circuit (performance improvement)	RTL design/Verification/Performance check SW development
	Image data communication	FPGA development 12G-SDI, PCIe (Gen3)	Architecture design/RTL design/Simulation/Verification/FPGA implementation/On-system verification
Others	**Automotive ASSP**	Ethernet switch for TSN	UVM environment creation/Expected value model development/Random verification by UVM
		Multi-gigabit ethernet PHY	Verification strategy planning Verification environment creation Functional verification(Direct verification)
	SSD	PCIe Gen4 additional functions LTSSM/PHY controller	Specifications creation SystemVerilog RTL design UVM verification environment creation and verification
	Edge computing	RISC-V CPU core	UVM verification environment creation Random verification by UVM ISS in-house development Expected values generation
Functional Safety	**Robot safety monitoring FPGA**	Functional expansion/reduction (IEC61508 SIL-2 compliance)	RTL design & verification
	CMOS image sensor	Digital Processing	Fault simulation
		Functional safety management	Configuration management Document management Traceability check (Reqtify)
		Functional safety consulting	Functional safety introduction/Functional safety process optimization/Functional safety assessment/audit/Evidence review
	Laser ranging sensor	Sensor data processing	Specifications creation RTL design & verification
	Laser controlled headlights	FPGA development	Reverse engineering Verification
	Automotive MCU	Functional safety consulting	Examples creation for Item Definition/HARA Customer training
			Documents creation and maintenance for ISO26262 process certification

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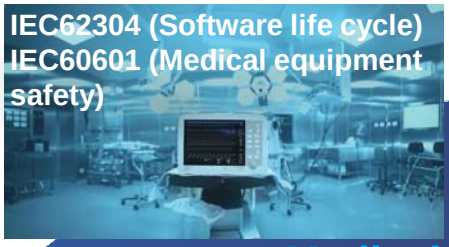
Vtech started considering LSI development compliance with international functional safety standards from an early stage since Vtech has focused on 3rd party verification for LSI development and has worked to improve design quality.
Vtech has a lot of FS Engineers/FS Managers qualified by TUV Rheinland, and offers high quality Functional Safety Services utilizing knowhow accumulated in LSI design and verification for diverse applications since Vtech was founded in 2003.



Medical

Automotive

Vtech offers Functional Safety Services for LSI development compliant with IEC61508.

IEC61508

Service robots

Agricultural machinery

Industrial machinery

Functional Safety Services Flow

Functional safety introduction support		Functional safety LSI development support
Preparation	Plan	Implementation
▪ GAP analysis ▪ Issues extraction	▪ PDCA Development process improvement	▪ Functional safety support for Concept, System design, and HW Development phases

Support Process Agency Services

- Bridge role for distributed development works
- Safety requirement specifications creation and management
- Change management
- (Reqtify, Redmine, etc.)
- Configuration management
- Verifications
- Document management
- Logic verification by use experience
- HW elements evaluation
- Interface for application not applicable to the standards
- Integration of safety related systems not compliant with the standard

Concept/System/LSI Design Support
for Functional Safety

Product Concept

Concept phase

Creates “Item Definition”
Performs “Hazard Analysis and Risk Assessment (HARA)”
Creates “Functional Safety Concept”

System phase

Creates “Technical Safety Concept”
(Technical Safety Requirements / Safety mechanism / System architecture design spec. / Technical Safety Concept / Safety analysis / Systematic failure avoidance / Work for HSI spec.)

LSI Logic Design phase

- Creates HW Spec.
  (HW architecture design/HW Safety Requirements spec./Safety mechanism spec.)
- Safety analysis (FMEA/FTA/FMEDA)
- Creates function/implementation spec.
- HW design
  (Coding for function/safety mechanism)

LSI Embedded SW Design phase

- Creates SW spec.
  (SW architecture design/SW Safety Requirements spec./Safety mechanism spec.
- Safety analysis (FMEA/FTA)
- Creates function/implementation spec.
- SW unit design and implementation
  (Coding for functional/safety mechanism)

LSI Logic Verification phase

LSI Embedded SW Verification phase

LSI System Verification phase

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LSI Verification Support for Functional Safety

Product Concept

Concept phase

System phase

LSI Logic Design phase

LSI Embedded SW Design phase

LSI Logic Verification phase

- Creates verification spec.
- Creates verification items list (for fault functional simulation/fault injection test)
- Creates verification environment
- Block verification
- System level verification
- Verification results reporting (HW architecture metric verification)

LSI Embedded SW Verification phase

- Creates verification spec.
- Creates verification items list (for fault functional simulation /fault injection test incl. coverage metric)
- Code analysis (Code review)
- Creates verification environment
- SW unit verification
- SW integration and verification
- Embedded SW test (HW in the loop, etc.)
- Verification results reporting

LSI System Verification phase

- Integration spec. and test strategy
- HW – SW integration and test
- System integration and test

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